REALIZATION OF THREE-PHASE ACTIVE RECTIFIER USING DSP56F803

Vladimír Minárik
Doctoral Degree Progeamme (2), FEEC BUT
E-mail: xminar13@stud.feec.vutbr.cz

Supervised by: Pavel Vorel
E-mail: vorel@feec.vutbr.cz

ABSTRACT

The article deals with a realization of a three-phase active rectifier in a laboratory programmable inverter. The control structure of the active rectifier was designed in Matlab Simulink and then implemented into the microprocessor Freescale DSP56F803 used in the laboratory inverter.

1. INTRODUCION

The progress of electronics brings next to many benefits also some unwanted influences. For example from the energetic view one of them is the burdening of the supply network system with joule losses and higher harmonic frequencies from the load currents. One way to eliminate these unwanted influences is the using of active rectifiers. The using of active rectifiers in electric drives brings the benefit of natural energy recuperation. The minimalization, digitizing and big contest pushing down the prices are the trends of nowadays. In this case one of the ways is the microprocessor realization of the active rectifier control. This article describes the implementation of the designed algorithm to the microprocessor and presents some of measurements realized on a real design.

2. CONTROL OF ACTIVE RECTIFIER

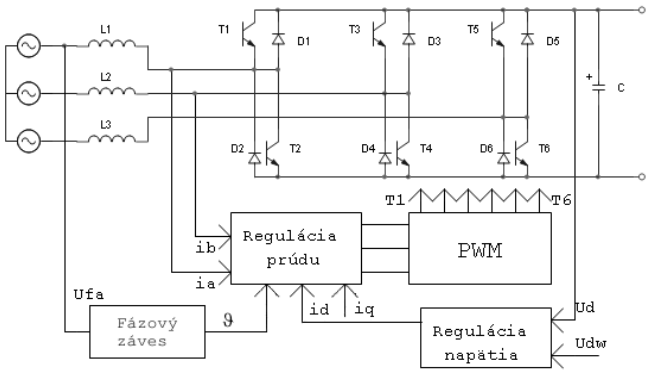

Fig. 1.: Schematic block of the three-phase rectifier control.

The active rectifier schematic is shown in fig. 1. The rectifier consists of a three-phase transistor bridge which is connected to the supply network thru operating inductors. The purpose of the control loops is to hold the desired voltage on the output capacitor higher than the maximal value of the phase to phase line voltage. Second, it must care to get the sine shape of the phase current taken from the supply network. And this must by independent on the energy flow direction - from or into the supply network. This is guaranteed using the cascade participation of the control loops with the master voltage loop and slave current loop. We need to ensure a synchronisation of the line voltage and the quasisinusoidal phase current controlled with the inverter. This way we control the phase shift between line voltage and current to a desired value (mostly we desire a zero phase shift). This phase control is realized with a phase locked loop.

2.1. DESIGN OF THE ALGORITHM

First we need to design the control algorithm of the active rectifier, before we start to write the program for the microprocessor. We have created this in MATLAB SIMULINK. It shows the fig. 2. The current control loop operates with DC values. These were transformed from real AC values using a Park and Clark transformation. Then an equivalent back transformation is necessary. The parameters in the simulation are equal to the real ones. We use the symmetric optimum method (SO) to design the parameters of controllers.

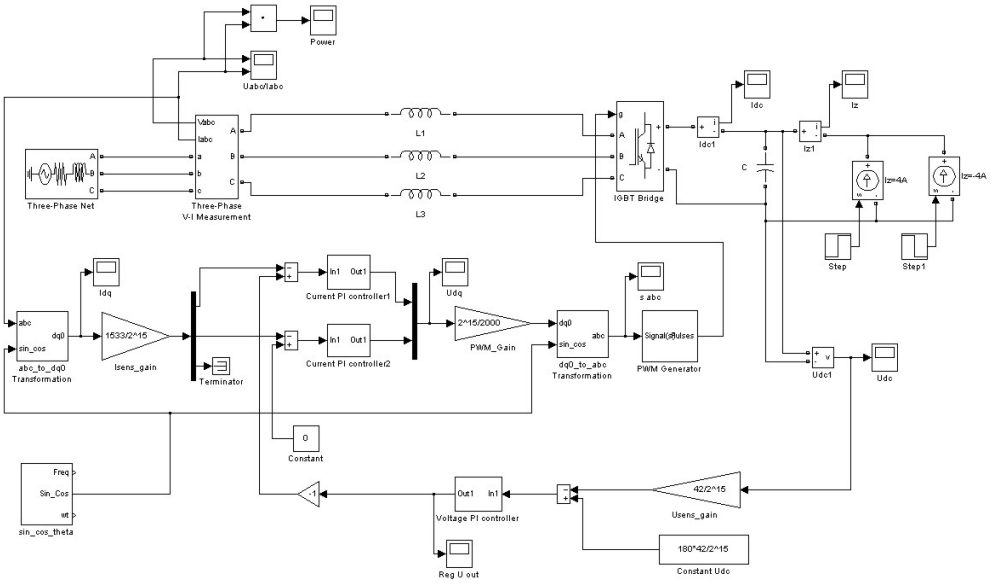

Fig. 2.: Simulation scheme of the rectifier in MATLAB Simulink.

3. DSP56F803

We implement the checkout simulated algorithm into the microprocessor. The 16-bit microprocessor DSP56F803 is a member of the DSP56800 core-based family of hybrid controllers. It can make as many as 40 MIPS at 80MHz core frequency. It includes many peripherals as two 4-chanel 12-bit AD converters, 6-chanel PWM modulator, four general purpose timers, sixteen multiplexed general purpouse I/O pins and so on. The program for the processor can by written in assembler or C programming language by the use of the pro-

gramming environment CodeWarrior. For the debugging of the program code to the microprocessor the JTAG/OnCE interface is used.

3.1. AD CONVERTER

Input current, output voltage and the voltage values for the phase locked loop are measured by the current and voltage transducer and then adapted to a desirable range of 0…±1.65V for the AD inputs. The order of the measured parameters is in the table 1. By using of Chanel List Register we can allocate the current inputs to the concrete samples. The AD module works in Simultaneous Mode. The inputs are measuring in Single-Ended Mode. But the accomplishment is always positive. We get the negative value by using the offset register. An over/under-voltage interrupt is generated by an overrun of the high or low voltage limit. The AD converter works at 5MHz and is synchronized by the TC2 timer with the PWM modulator.

Sample number	Channel number	Measurement parameter
0	0	I_b
1	2	U_b
2	4	U_{DC}
3	7	Potentiometer 1
4	1	I_a
5	3	U_a
6	5	-
7	6	Potentiometer 2

Table 1.: AD converter channels

3.2. PWM MODULATOR

The PWM modulator is configured as three complementary pairs, where we control only the switching period of the high transistors and the switching period of the low transistors is calculated. When generating complementary PWM signals, automatic deadtime insertion to PWM output pairs is possible to set. The PWM counter is an up-counter during an Edge-Aligned operation. In this mode the PWM highest output resolution is one IPBus clock cycle. The modulus (4000) is the period of the PWM output in PWM clock cycles (1). This means that the PWM modulator is working at 5kHz.

$$\text{PWM period} = \text{PWM modulus} \times \text{PWM clock period} \quad (1)$$

The log0 in the Fault0 input calls the interrupt which switchs-off the PWM outputs from the pins.

3.3. TIMERS

The primary use of TimerC2 is the synchronization of PWM modulator with AD converter. The counter input is connected to the PWM sync output and the output to the ADC sync input. TimerC1 is used to start the slow voltage control loop.The loop runs at 500Hz. The TimerC0 is used by the phase locked loop.

3.4. PROGRAM

At first the right succession of phases is tested and then the synchronization of DSP with the supply network is executed by the software phase locked loop. We used the original functions from Freescale for the Park, Clark transformations. These controllers are free to download on the Freescale sites. To generate values for the PWM the SVM modulation is used. The testing of fault signals is allways running on the background. The PWM_fault has the highest priority, which switchs-off the PWM outputs from the pins and saves the inverter. Other protection is the interrupt by over- or under-voltage of U_{DC}.

4. RESULTS OF MEASUREMENT

The most important parameter of the active rectifier is the sinusoidal shape of the taken current from the supply network, see fig. 3. The current is phased with the supply voltage. The DC voltage on the output of rectifier is shown in fig. 4. The drift of the output steady-state value is in the range of ±1 bit adjustment of the AD converter, what is ±1V.

a) b)

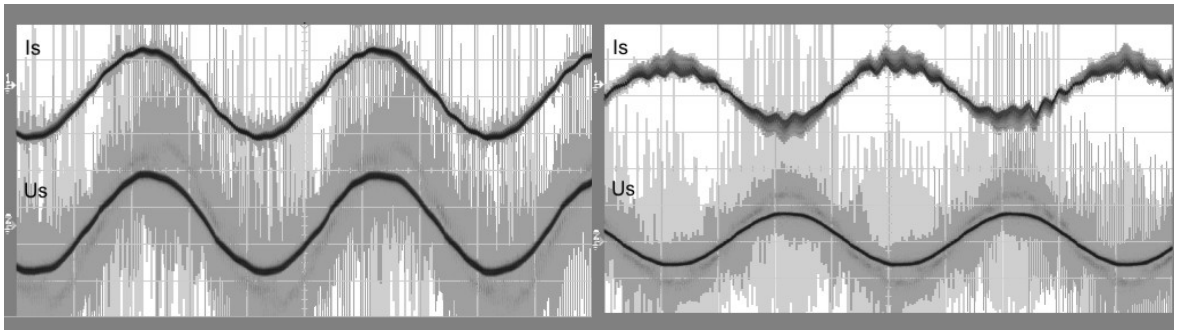

Fig. 3.: Active rectifier current: a) taken from the supply voltage b) by recuperation.

Fig. 4.: Active rectifier output voltage.

5. CONCLUSION

The three-phase active rectifier was designed using DSP56F803 digital signal controller in the laboratory programmable inverter. It is good to debug the algorithm in Matlab Simulink before the final implementation to the processor. The results of the measurement are shown in fig.3.,4.

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